Form PTO 1449 (Modified) DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 216692US2	SERIAL NO. 09/995,594
LIST OF REFERENCES CITED BY APPLICANT	APPLICANT Takashi YAMADA, et al.	
	FILING DATE November 29, 2001	GROUP 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
TD	AM	10-303385	11/13/98	JAPAN (with English Abstract)		X
TD	AN	8-316431	11/29/96	JAPAN (with English Abstract)		X
TD	AO	7-106434	04/21/95	JAPAN (with English Abstract)		X
TD	AP	11-238860	08/31/99	JAPAN (with English Abstract)		X
TD	AQ	2000-91534	03/31/2000	JAPAN (with English Abstract)		X
TD	AR	2000-243944	09/08/2000	JAPAN (with English Abstract)		X
TD	AS	8-17694	01/19/96	JAPAN (with English Abstract)		X
TD	AT	11-17001	01/22/99	JAPAN (with English Abstract)		X
TD	AU	2000-269460	09/29/2000	JAPAN (with English Abstract)		X
TD	AV	2001-196556	07/19/2001	JAPAN (with English Abstract)		X

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

TD	AW	Robert HANNON, et al., 2000 Symposium on VLSI Technology Digest of Technical Papers, pages 66-67, "0.25 μm MERGED BULK DRAM AND SOI LOGIC USING PATTERNED SOI", June 13, 2000
TD	AX	M. SATO, et al., 2000 Symposium on VLSI Technology Digest of Technical Papers, pages 82-83, "TRANSISTOR ON CAPACITOR (TOC) CELL WITH QUARTER PITCH LAYOUT FOR 0 13 μm DRAMS AND BEYOND", June 13, 2000
	AY	
	AZ	

Examiner [signature] Date Considered 3/21/03

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.